FIG. 1

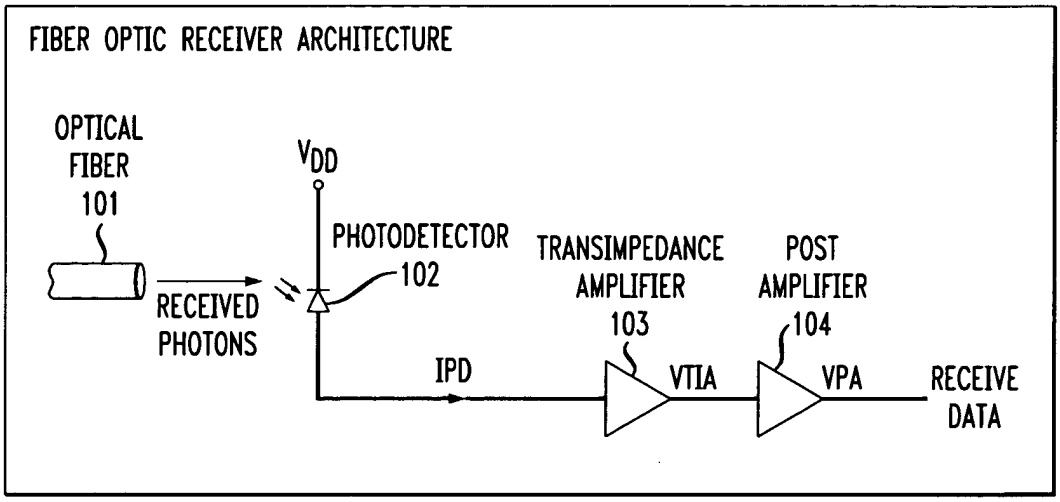
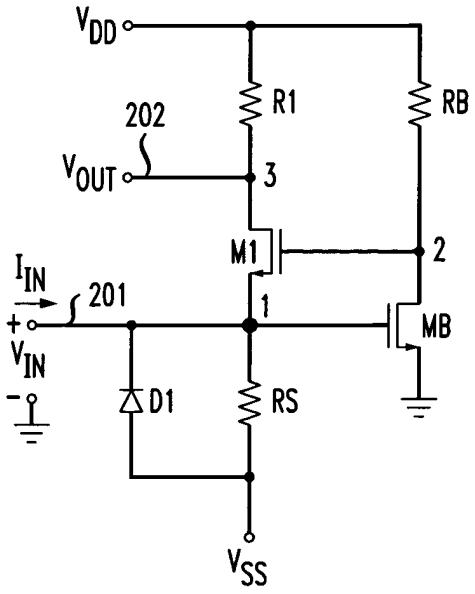


FIG. 2

PRIOR ART

SCHEMATIC DIAGRAM OF THE REGULATED CASCODE (RGC) INPUT STAGE



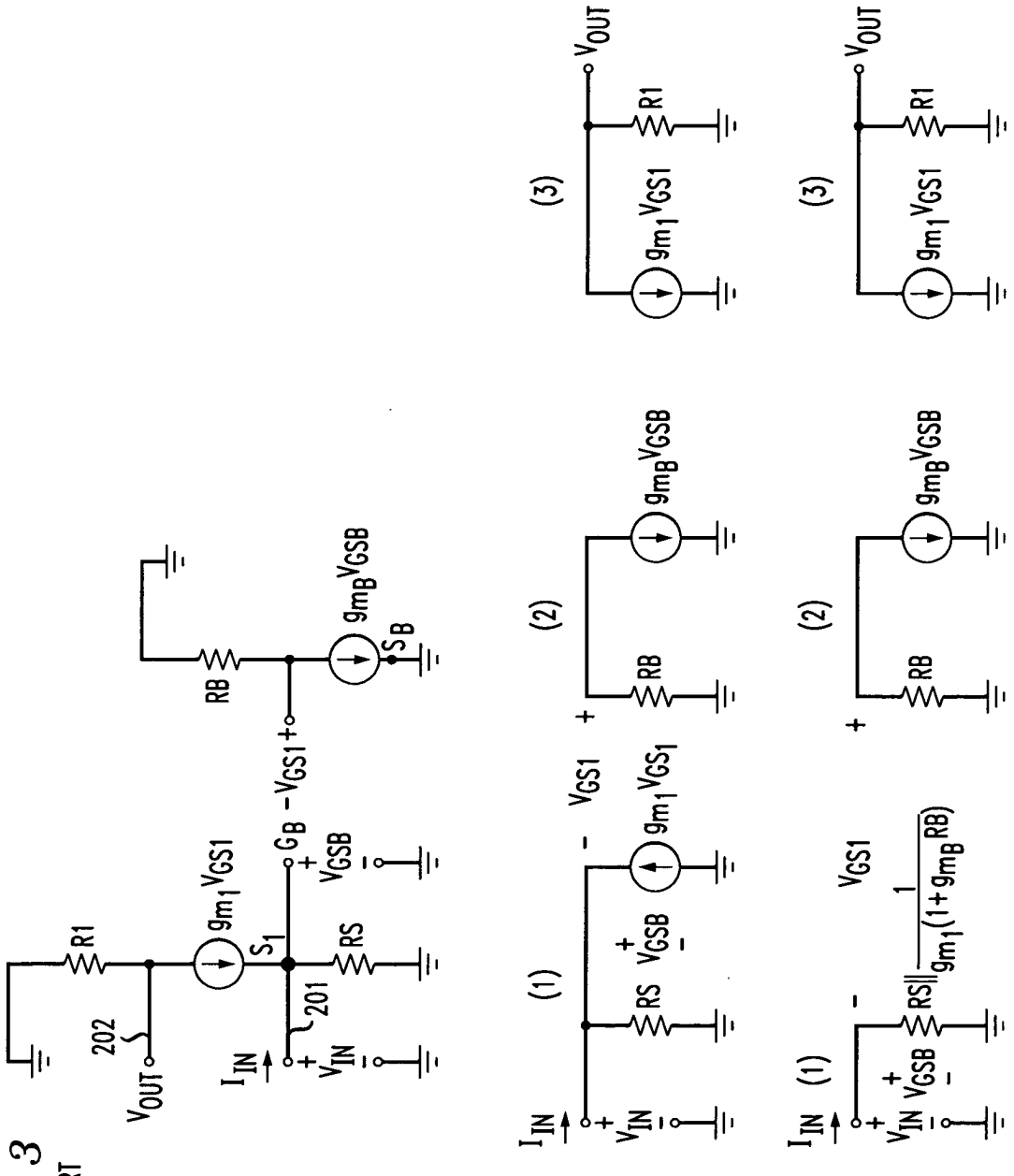
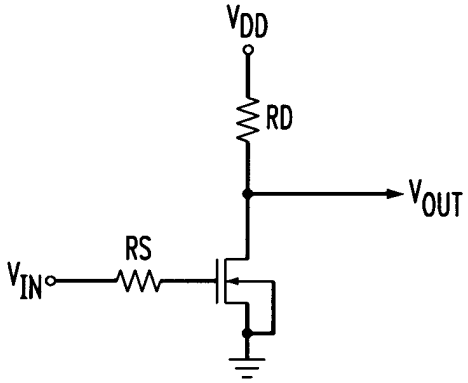


FIG. 3
PRIOR ART

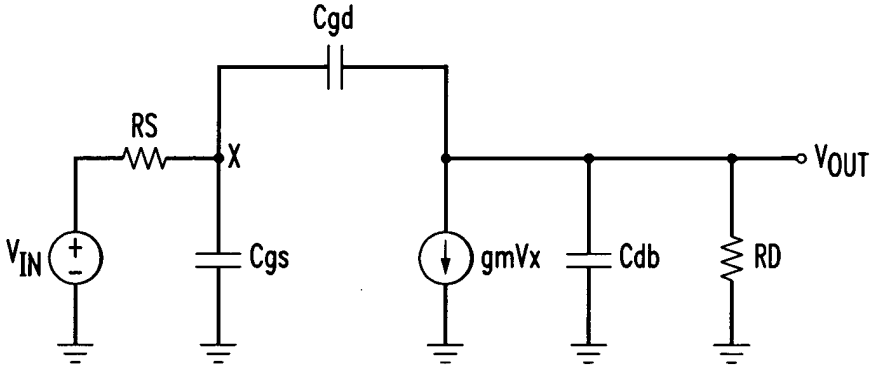
FIG. 4
PRIOR ART

(a)



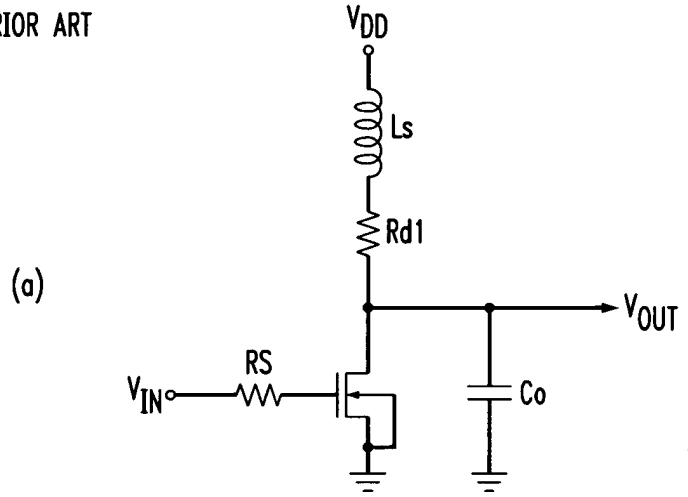
COMMON SOURCE STAGE AMPLIFIER

(b)

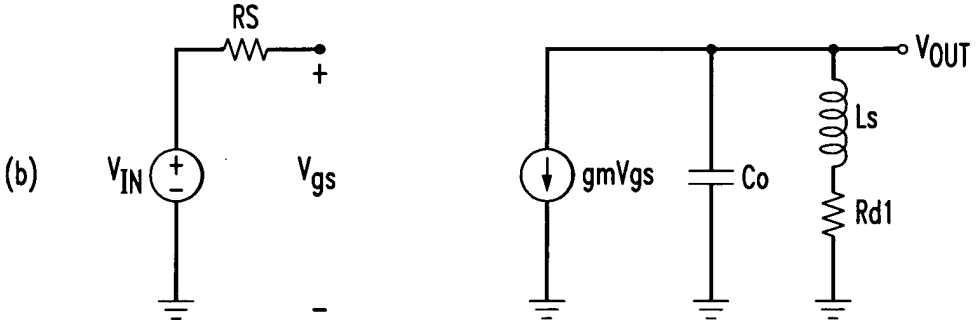


HIGH FREQUENCY MODEL OF A COMMON SOURCE STAGE

FIG. 5
PRIOR ART



TYPICAL SHUNT PEAKED AMPLIFIER



EQUIVALENT SMALL SIGNAL MODEL FOR CIRCUIT IN FIGURE 5a

FIG. 6

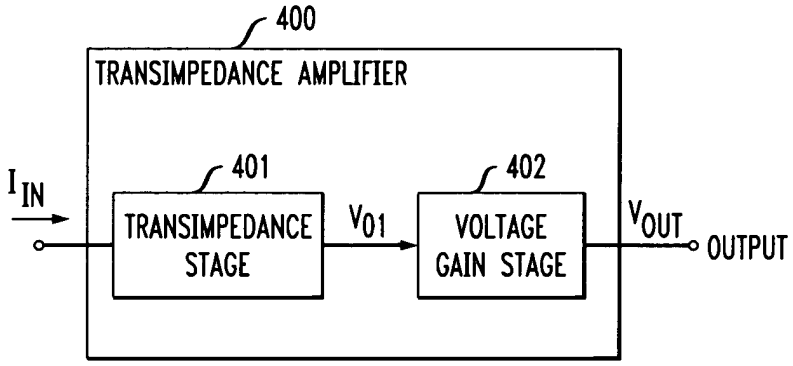
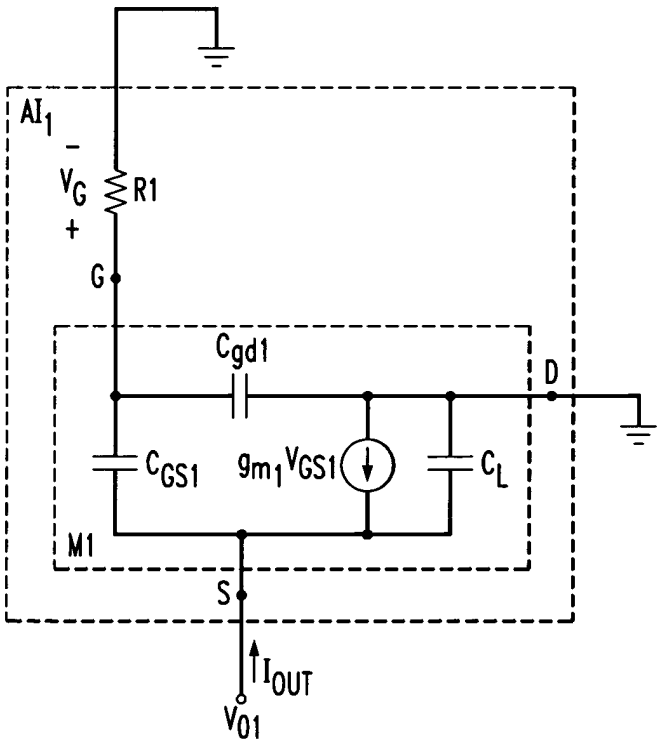

400
TRANSIMPEDANCE AMPLIFIER
401
402
I_{IN}
TRANSIMPEDANCE STAGE
V_{01}
VOLTAGE GAIN STAGE
V_{OUT}
OUTPUT

FIG. 8


AI_1
V_G
R1
G
C_{gd1}
D
C_{GS1}
$g_{m1}V_{GS1}$
C_L
M1
S
I_{OUT}
V_{01}

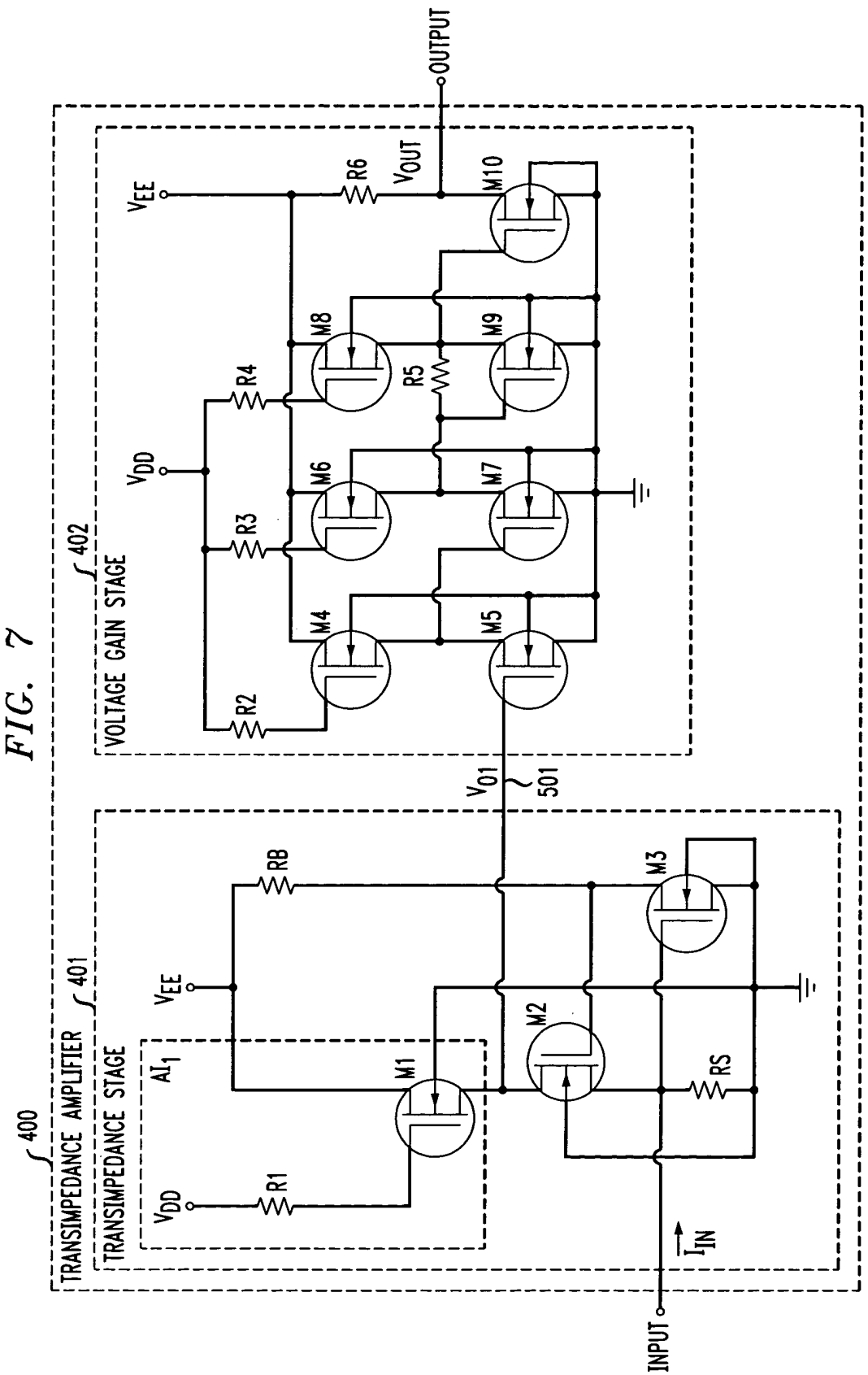
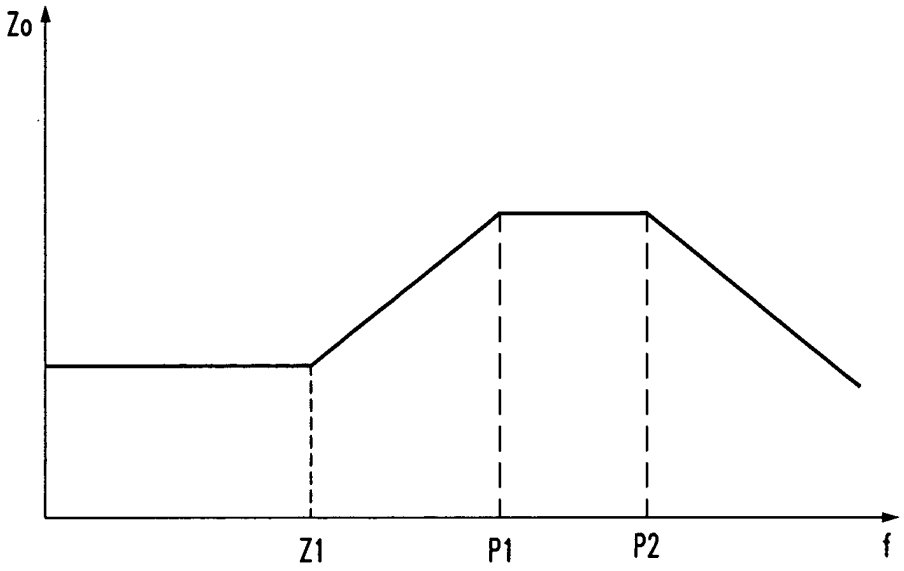

OUTPUT
INPUT
400
TRANSIMPEDANCE AMPLIFIER
401
TRANSIMPEDANCE STAGE
402
VOLTAGE GAIN STAGE
501
V_{EE}
V_{DD}
V_{OUT}
V_{01}
AI_1
I_{IN}
R1
R2
R3
R4
R5
R6
RB
RS
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10

FIG. 7

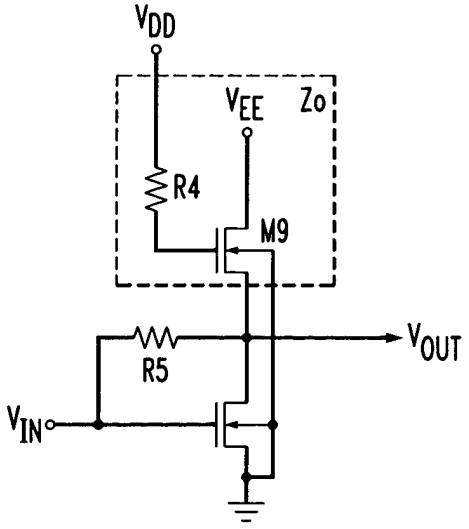
FIG. 9



GRAPH OF Zo VERSUS FREQUENCY

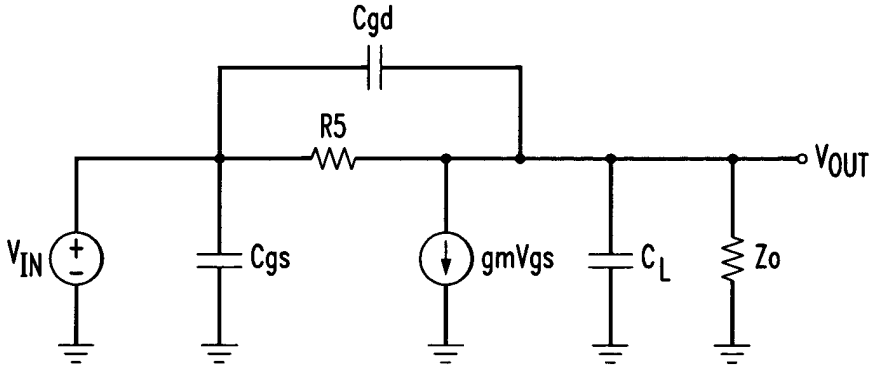
FIG. 10

(a)



COMMON SOURCE STAGE WITH FEEDBACK RESISTOR

(b)



HIGH FREQUENCY MODEL FOR COMMON SOURCE STAGE WITH FEEDBACK RESISTOR